Amendment t the Abstract:

The Abstract has been amended. A revised Abstract is attached.

ABSTRACT

~~To provide a printed circuit board, a buildup substrate and a method of manufacturing the printed circuit board capable of curbing a transmission loss thereof at a desired frequency.~~

A printed circuit board having a multilayer substrate~~-~~, a via hole penetrating the multilayer substrate, a surface wiring wired on the surface of the multilayer substrate and connected to an end which is one end of the via hole, at least one inner layer wiring formed inside the multilayer substrate and connected to a portion other than upper and lower ends of a conductive part of the via hole, and a current-carrying element connected to an end having no surface wiring connected thereto on an opposite side to the end, and wherein the current-carrying element has an electrical length by which a value of an impedance at a predetermined frequency on seeing the current-carrying element side from a connection point between the inner layer wiring and the via hole closest to the end is larger than a value of the impedance on seeing the end from the connection point in the case where the current-carrying element is nonexistent.

Respectfully submitted,

Allan Ratner, Reg. No. 19,717
Attorney for Applicants

AR/fp

Attachment: Abstract

Dated: September 30, 2003

The Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. **18-0350** of any fees associated with this communication.	**EXPRESS MAIL: Mailing Label Number: EV 351 885 295 US** **Date of Deposit: September 30, 2003** I hereby certify that this paper and fee are being deposited, under 37 C.F.R. § 1.10 and with sufficient postage, using the "Express Mail Post Office to Addressee" service of the United States Postal Service on the date indicated above and that the deposit is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450. Kathleen Libby **KATHLEEN LIBBY**

ABSTRACT

A printed circuit board having a multilayer substrate, a via hole penetrating the multilayer substrate, a surface wiring wired on the surface of the multilayer substrate and connected to an end which is one end of the via hole, at least one inner layer wiring formed inside the multilayer substrate and connected to a portion other than upper and lower ends of a conductive part of the via hole, and a current-carrying element connected to an end having no surface wiring connected thereto on an opposite side to the end, and wherein the current-carrying element has an electrical length by which a value of an impedance at a predetermined frequency on seeing the current-carrying element side from a connection point between the inner layer wiring and the via hole closest to the end is larger than a value of the impedance on seeing the end from the connection point in the case where the current-carrying element is nonexistent.